Description

The FX-427 is a precision quartz-based frequency translator used to translate 1 to 4 selected input clocks as low as 8 kHz to an integer multiple as high as 850 MHz. The FX-427's superior jitter performance is achieved through the filtering action of the on-board voltage-controlled SAW oscillator (VCSO) and integrated loop filter. Two low-jitter outputs are provided. Monitoring and control functionality are also standard features.

Features

- Quartz-based PLL for Ultra-Low Jitter
- Frequency Translation up to 850 MHz
- Accepts 4 externally-muxed clock inputs
- LVCMOS/LVDS/LVPECL Inputs Compatible
- Differential LVPECL Outputs
- Lock Detect
- Output Disable
- 20.3 x 13.7 x 5.1 mm surface mount package
- Compliant to EC RoHS Directive

Applications

- Wireless Infrastructure
- 802.16 BTS
- 10 Gigabit FC
- 10GbE LAN / WAN
- OADM and IP Routers
- Test Equipment

Block Diagram

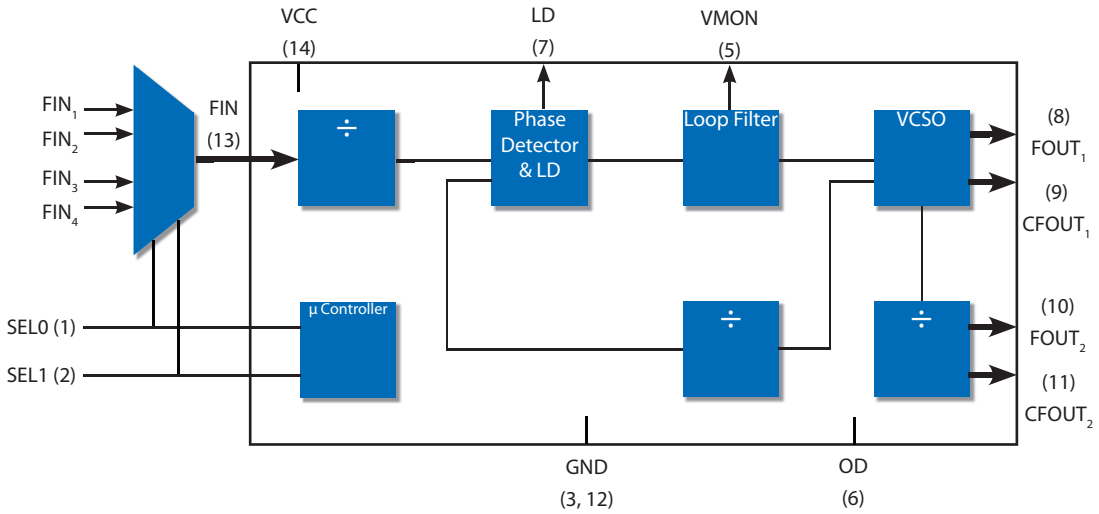

Figure 1. Functional block diagram

Performance Specifications

Table 1. Electrical Performance

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency [1, 2, 3]					
Input Frequency	F_{IN}	0.008		200	MHz
Capture Range	APR	±40			ppm
Output Frequency - Primary	F_{OUT1}	500		850	MHz
Output Frequency - Secondary	F_{OUT2}	125		850	MHz
Supply					
Voltage [2, 3]	V_{CC}	3.13	3.3	3.46	V
Current (No Load)[3]	I_{CC}		140	180	mA
Input Signal					
LVCMOS	F_{IN}		LVCMOS		
LVDS [2, 3, 7]	F_{IN}		LVDS		
LVPECL	F_{IN}		LVPECL		
Differential Output (Options F and P) [2, 3, 4, 5]					
Common Mode Output Voltage	V_{OCM}	V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	V
DC Output High Voltage	V_{OH}	V_{CC}-1.085	V_{CC}-0.950	V_{CC}-0.880	V
DC Output Low Voltage	V_{OL}	V_{CC}-1.830	V_{CC}-1.7	V_{CC}-1.620	V
Peak to Peak Output Voltage	V_{P-P}		700		mV p-p
Rise TIme	t_R		0.5		ns
Fall Time	t_F		0.5		ns
Symmetry	SYM	45	50	55	%
SSB Phase Noise, Fout = 155.52/622.08 [5, 6]					
10Hz Offset	Φ_n		-64/-27		dBc/Hz
100Hz Offset	Φ_n		-95/-55		dBc/Hz
1kHz Offset	Φ_n		-123/-123		dBc/Hz
10kHz Offset	Φ_n		-143/-110		dBc/Hz
100kHz Offfset	Φ_n		-146/-130		dBc/Hz
1 MHz Offset	Φ_n		-146/-146		dBc/Hz
10 MHz Offset	Φ_n		-146/-146		dBc/Hz
Jitter Generation [5, 6]					
155.52 MHz (12kHz - 20MHz BW)	Φ_J		0.30		ps RMS
622.08 MHz (12kHz - 20 MHz BW)	Φ_J		0.12		ps RMS
Operating Temperature (Options C of F) [1, 3]	T_{OP}	0 to 70 or -40 to 85			ºC

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 2).
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 3).
5. Not tested in production, guaranteed by design, verified at qualification.
6. The FX-427 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.
7. LVCMOS input signal levels are valid for input frequencies < 100 MHz.

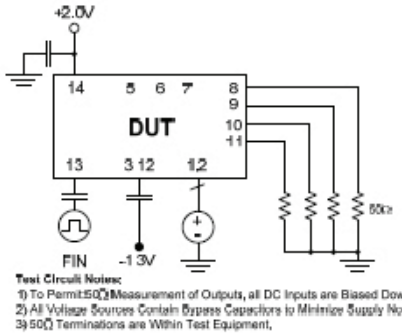

Figure 2. Test Circuit

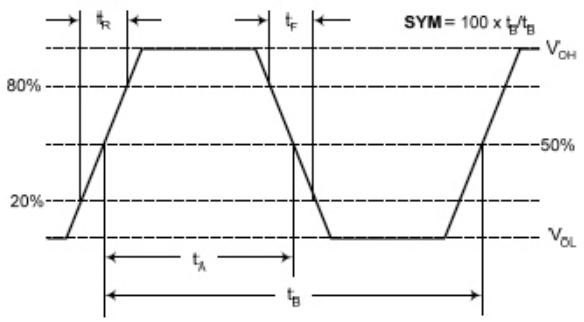

Figure 3. LVPECL Waveform

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DD}	6	V
Storage Temperature	T_{STR}	-55 to 125	ºC
Soldering Tewmp/TIme	T_{LS}	260/40	ºC/sec

Reliability

The FX-427 is capable of meeting the following qualification tests

Table 3. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitrry has been designed into the the FX-427, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance=1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes

Table 4. Predicted ESD R$atings

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

Reflow Profile

Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 ºC/sec Max
Time Above 217 ºC	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 ºC	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 ºC/sec Max

The FX-427 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-427 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-427 has been designed for pick and place reflow soldering. The FX-427 may be reflowed once and should not be reflowed in the inverted position.

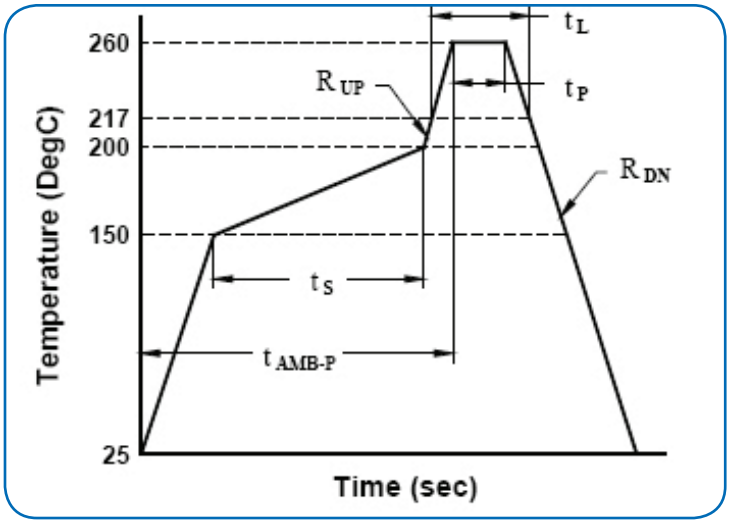

Figure 4. Suggested IR Profile

Tape and Reel

Table 6. Tape and Reel Information												
Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
32	14.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	200

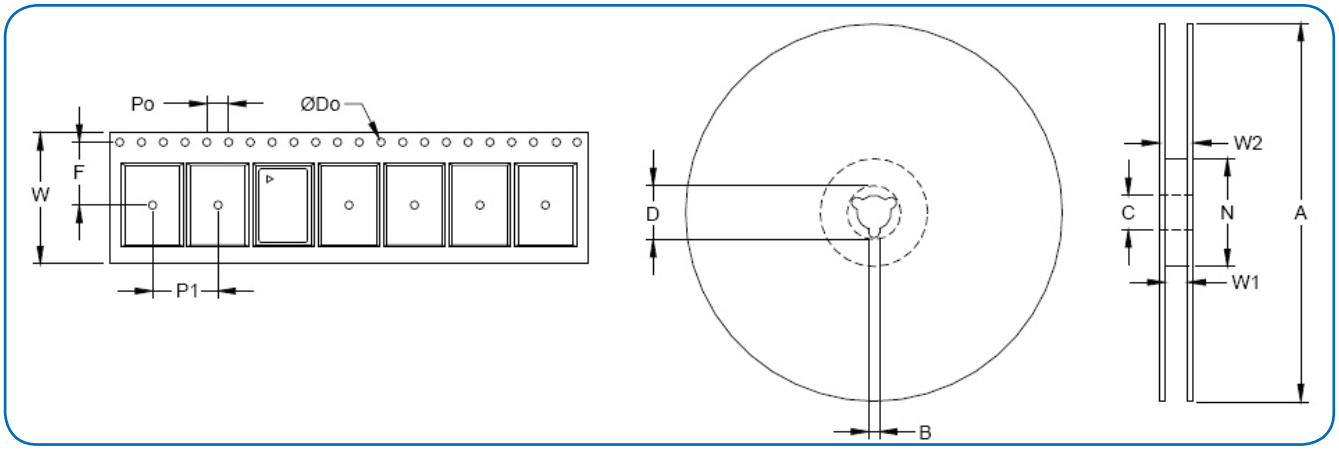

Figure 5. Tape and Reel

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Pin Configuration

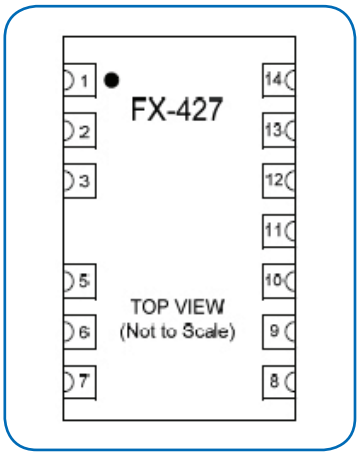


Figure 6. Pin Configuration

Table 7. Pin Functions

Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVCMOS	Frequency Select - see table 3
2	SEL1	I	LVCOMS	Frequency Select – see table 3
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O		VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and <3.0V. The input frequency may be out of range if the voltage exceeds these levels
6	OD	I	LVCMOS	Output Disable Disabled = Logic "1" Enabled = Logic "0" or no connect
7	LD	O	LVCMOS	Lock Detect Locked = Logic "1" Loss of Lock = Logic "0"
8	FOUT1	O	LCPECL	Frequency Output – Primary
9	CFOUT1	O	LVPECL	Complimentary Frequency Output - Primary
10	FOUT2	O	LVPECL	Divided-Down VCSO/VCXO Output, or Disabled
11	CFOUT2	O	LVPECL	Complimentary Divided-Down VCSO/VCXO Output, or Disabled
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVCMOS or LVPECL	Input Frequency – AC Coupled
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

LVCMOS input signal levels are valid for input frequencies < 100 MHz.

Table 8. Control Logic (LVCMOS)

SEL 0	SEL 1	CLock Input
0	0	FIN_1
0	1	FIN_2
1	0	FIN_3
1	1	FIN_4

FX-427 Outline Diagram and Pad Layout

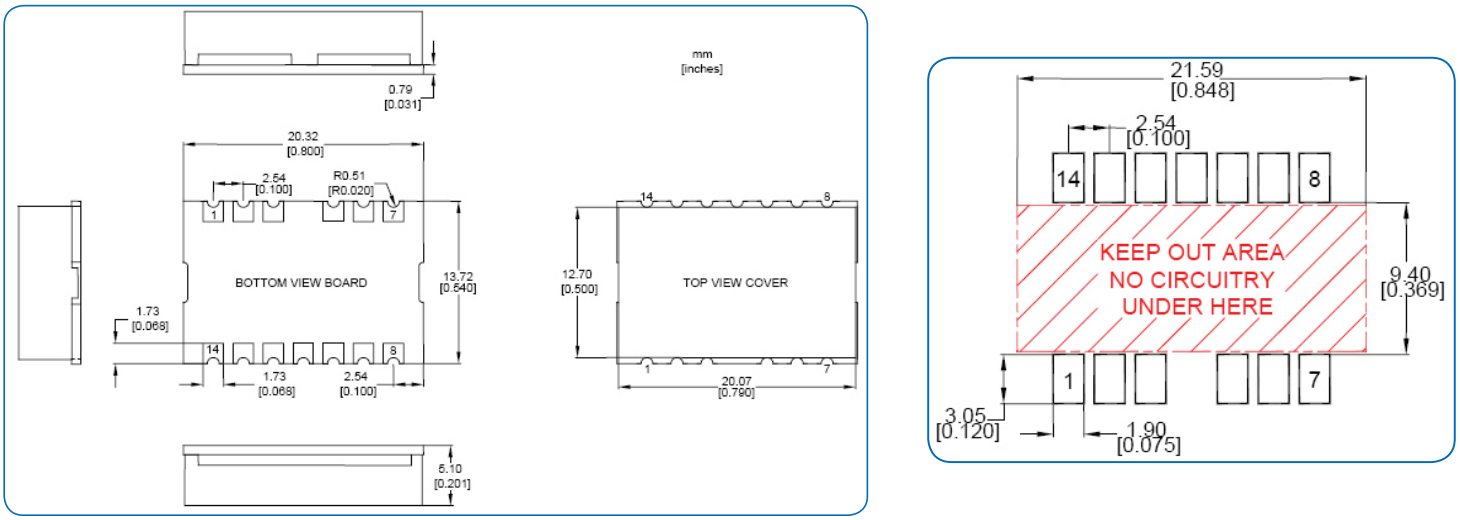
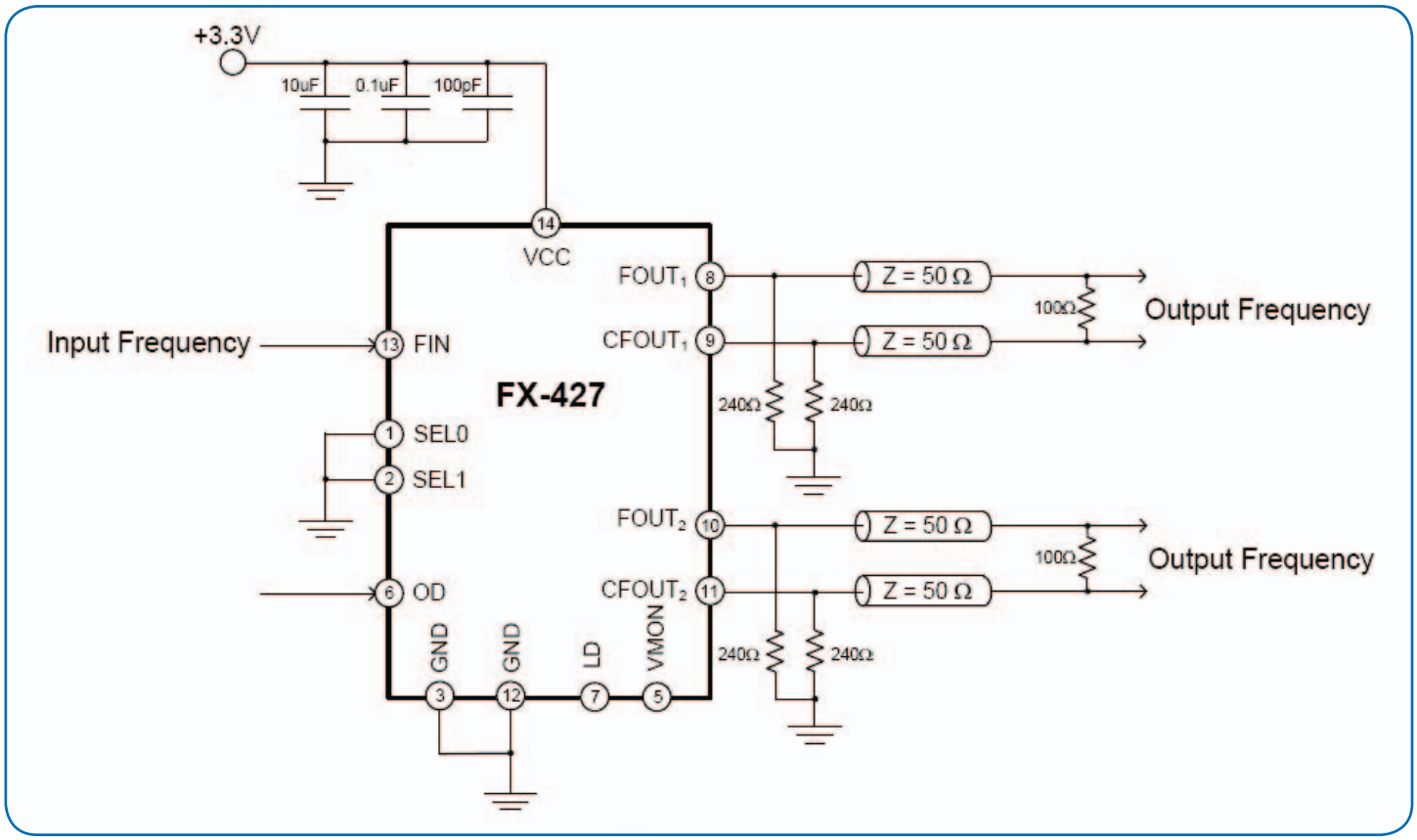


Figure 7. Outline and Pad Layout

Suggested Output Load Configurations



LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.

Ordering Information

Table 9. Standard Frequencies

0.0008	AN	3.088	B6	19.6608	DB	41.0889	KM	78	LH	200	NE	647.2508	PK
0.001	A1	3.24	BL	19.699	DK	41.6571	KP	78.125	K3	200.192	N6	649.9703	PF
0.002	AR	3.25	BC	19.719	DH	41.66	LM	78.6432	K5	201.416	N1	657.4219	PB
0.0032	AG	3.375	BH	19.9219	ED	41.8329	KT	79.6875	KG	212.5	NF	665.6256	PC
0.004	A2	3.84	B7	20	E2	42	JB	80	K9	219.4296	NL	666.5143	P5
0.008	A3	4	BN	20.1416	E3	42.0102	KV	80.5664	KJ	240	NR	669.1281	R2
0.0095	AU	4.096	B5	20.48	E4	42.5	JC	82.1777	KL	243	NC	669.3266	R3
0.01	A6	5	C6	20.5444	EF	42.66	JZ	82.944	K6	245.76	N9	669.6429	R1
0.0156	AL	5.12	CD	20.7135	E1	44.2095	KX	83.3143	KN	250	NT	670.8386	R7
0.0157	AD	6.144	CG	20.8286	EB	44.4343	LF	83.6658	KR	252.5714	NJ	672	RT
0.0158	AC	6.2914	CC	20.8286	EG	44.6218	JW	84.0203	KU	256	NK	672.1563	TX
0.016	A4	6.2915	CF	20.9165	EH	44.736	J3	86.6854	LJ	262.144	NB	672.1627	R5
0.024	BX	6.312	C7	21.0051	EJ	44.928	JE	88.4191	KW	292.5714	NN	673.4566	RA
0.025	BR	6.48	C2	22	E9	45.1584	JG	95.7	LK	300	PT	684.2554	R9
0.032	BW	6.75	CB	22.1048	EK	45.824	JM	97.5	KE	307.2	RX	687.7	TV
0.04	AP	7.68	C9	22.2171	E5	46.0379	LG	100	L8	311.04	P1	690.5692	R4
0.0441	AA	7.776	C5	22.5792	E8	46.72	JK	105	L6	312.5	PU	693.4688	RV
0.048	AB	8.192	C3	24	EC	46.875	JY	106.25	L9	318.75	PV	693.483	R6
0.0481	AV	9.216	CH	24.576	E6	48	JV	108	LA	320	PP	693.75	R8
0.05	BT	9.72	C8	24.704	E7	49.152	J7	110	L1	322.2657	PW	696.3906	RW
0.064	A5	9.75	CE	25	F7	49.408	J2	112	L2	328.711	PX	696.4219	TY
0.08	A9	9.8304	C1	25.1658	F8	50	JD	114	L3	333.2572	PY	704.3806	TG
0.1	AH	10	C4	25.6	F6	50.048	KD	120	LC	334.6633	RB	707.3527	TC
0.128	AX	10.23	DP	25.92	F2	51.2	LL	122.88	LB	336.0814	RC	710.9486	T2
0.243	A8	10.24	DM	26	F3	51.84	J4	124.416	L7	353.6764	RD	712.52	TW
0.256	AM	10.4143	DV	27	F4	52	JP	125	L4	368.64	RY	716.5732	T1
0.32	AW	10.4582	DU	27.648	FB	53.33	JU	130	LD	375	RF	718.75	T5
0.384	AY	10.4872	DN	28.704	F1	54.746	JL	139.264	L5	382.8	RU	719.7344	T3
0.4	AF	10.949	DG	29.4912	F5	55	JX	150	M8	400	RR	737.28	TL
0.48	AK	10.95	DJ	29.5	F9	60	JR	150.144	M6	409.6	RE	739.2	TT
0.5	BP	11.184	DF	30	HE	61.38	KY	153.6	MA	491.52	PM	748.0709	T6
0.512	AJ	12.288	D8	30.72	H1	61.44	J5	155.52	M2	500	RK	750	T7
0.6555	AE	12.3077	DY	30.88	HF	62.208	J8	156.25	M3	531	PH	768	TN
0.772	AT	12.352	D1	31.25	H8	62.5	J9	159.375	M7	531.25	P8	777.6	T4
0.96	A7	12.8	D2	32	H2	62.9145	LE	160	M1	568.9286	PJ	779.5686	T8
1	BB	13	D3	32.768	H3	63.36	JJ	161.1328	M4	569.1964	P9	780.881	TD
1.024	B2	13.5	DT	33	H7	63.8976	JN	164.3555	M9	588	RH	781.25	T9
1.215	BU	14.8352	DL	33.333	HC	64	JT	166.6286	M5	595.056	PL	796.875	TB
1.2288	BK	15	D4	34.368	H6	64.152	JH	167.3316	N2	600	PR	800	TK
1.25	BG	15.0336	DR	34.56	HB	65.536	J6	168.0407	N3	614.4	RG	805.6641	TA
1.3333	BF	15.36	DW	36.864	HG	66	JA	170	N4	622.08	P2	809.0635	TE
1.5	BE	16	D9	37.056	H4	70	KB	172.5	NU	624.6938	PD	819.2	TH
1.536	BV	16.384	D5	37.125	H9	70.656	KC	173.3707	ND	624.7048	P6	821.7773	TF
1.544	B3	17.184	DE	37.5	HK	71.61	KF	173.4375	NP	625	P3	850	TJ
1.92	B1	18.432	D7	38.88	H5	73.728	K8	176.8382	NA	627.3296	P7		
2	B8	18.528	DC	39.0625	HH	74.125	K1	182.016	N8	629.9878	PA		
2.048	B4	18.75	EE	39.3216	HD	74.1758	KA	182.8571	NM	637.5	PG		
2.304	BD	19.2	DD	39.8438	HJ	74.25	K7	184	NG	640	PN		
2.4576	BJ	19.3927	DX	40	JF	75	KH	184.32	NH	644.5313	P4		
2.5	BM	19.44	D6	40.2831	KK	76.8	K4	187.5	N5	645.12	RJ		
2.5575	B9	19.5313	DZ	40.96	J1	77.76	K2	195	N7	647.2394	PE		

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Ordering Information

F X - 4 2 7 - X X X - X X X X X

Power Supply
D: 3.3 Vdc

Output
F: LVPECL
P: LVDS

Temperature Range
C: 0 to 70ºC
F: -40 to 85ºC

Input Frequency
(A3 to RR)

Ouptut Frequency
(RK to TJ)

Second Output
A: Divide by 1
B: Divide by 2
C: Divide by 4
K: Disabled

EXAMPLE: FX-427-DFF-A3P2C
FX-427, 3.3V, LVPECL output, -40° to +85°C, FIN1 = 8 kHz, FOUT1 = 622.08 MHz, FOUT2 = 155.52 MHz.

EXAMPLE: FX-427-DFC-SSP2B, S = 2.048 MHz, 19.44 MHz, 77.76 MHz
FX-427, 3.3V, LVPECL output, 0° to 70°C, FIN1 = 2.048 MHz, FIN2 = 19.44 MHz, FIN3 = 77.76 MHz, FOUT1 = 622.08 MHz, FOUT2 = 311.04 MHz

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