# 25.000 MHz Jitter Attenuation Reference Design

While total jitter requirements in Ethernet applications are not as stringent when compared with SONET/SDH requirements, it is still often the case that a derived or recovered clock in Synchronous Ethernet proves to have excess jitter to support line and central clock card requirements. A "jitter attenuation" or "clock clean-up" is required, and for these applications Vectron has developed the CD-700-SynchE, a small 5x7mm, competitively priced, low jitter solution. This application note includes a recommended loop filter design, and shows the jitter and phase noise improvement performance when a jittered signal is applied, using the loop filter design shown in Figure 1.

The CD-700 includes a phase detector, op-amp, and a VCXO with associated divide-by. As a classic analog PLL it can be used to clean up a jittered or noisy signal, and it eliminates the discrete jumps associated with digital PLL's. The 50MHz VCXO has wide pull capabilities meeting 100ppm capture or APR range, needed per Ethernet standards. Also it has excellent phase noise performance, which is achieved by dividing the already low phase noise 50MHz VCXO output by 2 to provide a 25.00MHz signal. The CD-700 provides 2 separate 25 MHz outputs; when a jittered 25MHz signal is applied to DATAIN a clean 25MHz signal can be derived from both OUT2 as well as RDATA.

In addition, the CD-700 includes a loss of signal (LOS) which detects when the input frequency has shut down and acts as an alarm. The LOS goes from a logic 0 to a logic 1 after 128 missing cycles on the input. The benefit of this feature is twofold; it can also be used to set the VCXO frequency by connecting LOS to LOSIN, and used as an alarm.

The recommended loop filter is shown in Figure 1. This design was optimized for low jitter peaking, < 0.1 dB typical, and to maximize phase margin which is 86 degrees typical. The loop bandwidth is wide enough to allow proper locking and wander tracking but rejects out high frequency noise. The design in Figure 1 was used to demonstrate the clean-up capability shown in Figures 2, 3, 4 and 5 and is recommended for customer applications .

## Block Diagram

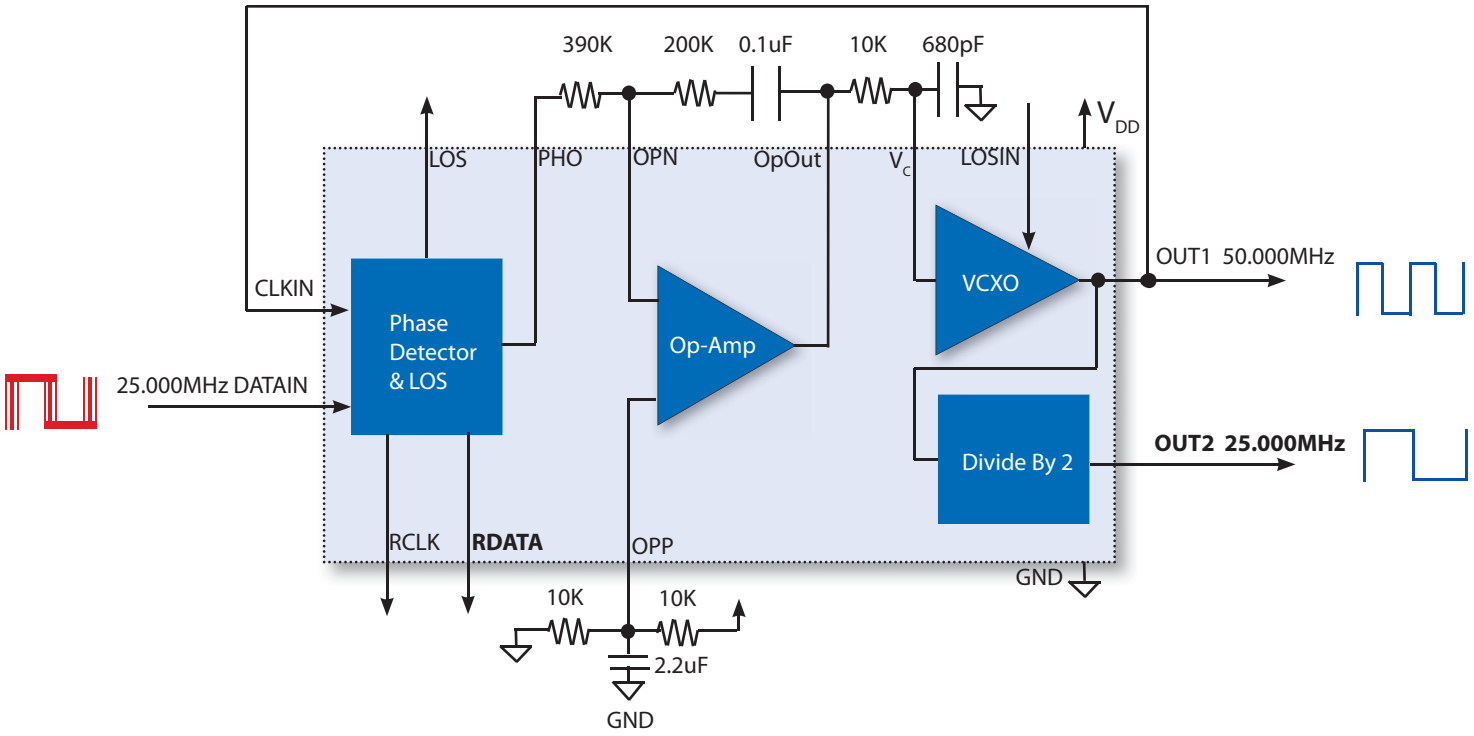


**Figure 1**
The loop filter design has a 1kHz simulated BW

The CD-700's clean-up performance was characterized by measuring the 25MHz input and 25MHz output clock jitter, a time domain function, using a Wavecrest SIA3300C. As a minimum, 10K edges should be sampled in order to provide a realistic peak-peak value and 500K edges were sampled to provide robust results.

The CD-700 was injected with a noisy 25MHz clock source which has 1.954ns peak-peak Period Jitter, shown in Figure 2. The CD-700's output was measured and resulted in 19.867ps peak-peak Period Jitter - almost a 100 fold improvement - see Figure 3. The alternate 25MHz clock source, RDATA, has 22.526ps peak-peak Period Jitter as shown in Figure 4.

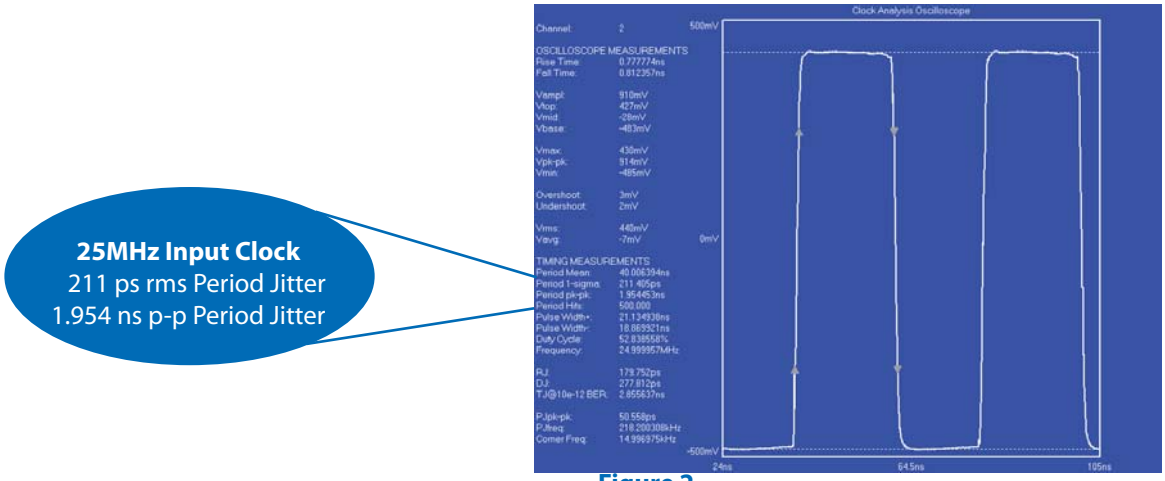


**Figure 2**
Jittered 25MHz Input Clock

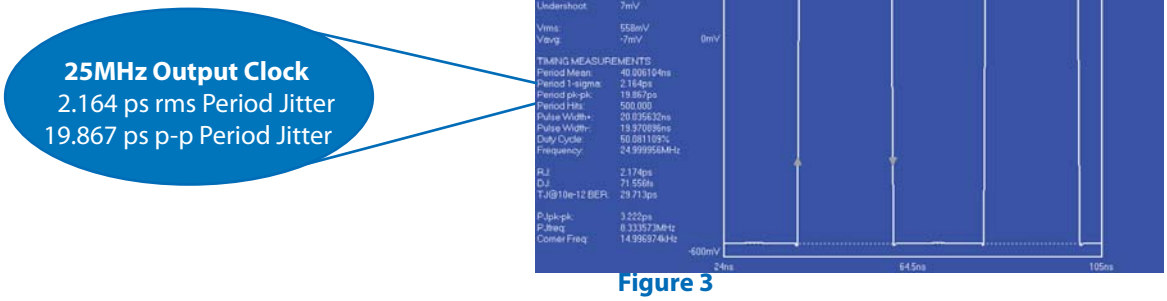


**Figure 3**
Clean 25MHz OUT2 Clock

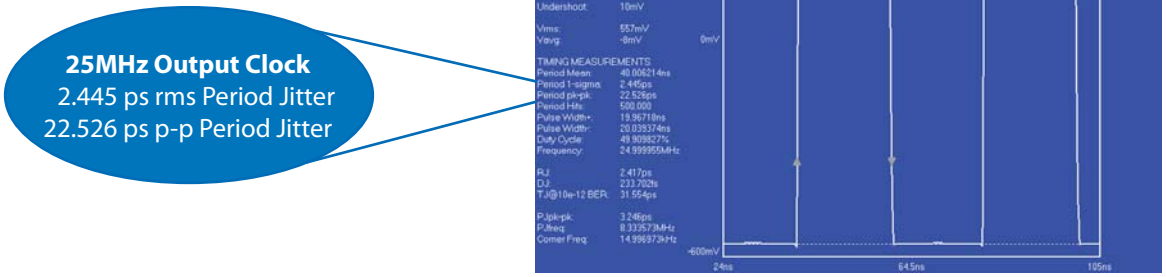


**Figure 4**
Clean 25MHz RDATA Clock

An Agilent E5052B was used to characterize the CD-700's clean-up performance in the frequency domain, offering another perspective. The CD-700 was injected with a noisy 25MHz clock source with a broadband noise of about -110dBc/Hz, as shown in figure 5. The CD-700 output was measured and compared, also in figure 5, which results in a 40-50dB improved floor performance.

For applications requiring 2 separate 25MHz clocks, RDATA can also be utilized but optimum performance is derived by using OUT1

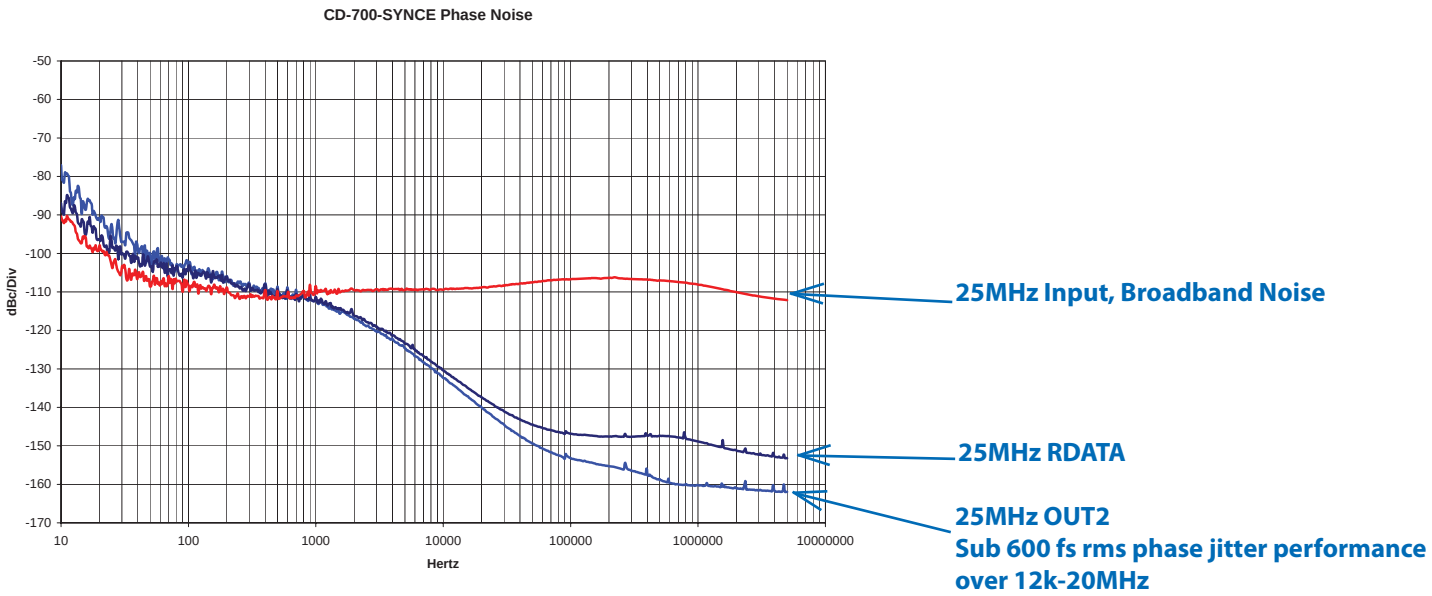


**Figure 5**
**Phase Noise Plot comparing Input to Output Phase Noise**

The CD-700 is a cost effective solution which will significantly reduce jitter in 25.000 MHz Synchronous Ethernet applications, meeting a 600fs rms phase jitter spec over the 12kHz to 20MHz bandwidth. Added benefits include reduced design time, guaranteed performance, and a reduction in board space and component cost compared to discrete PLL's.

Vectron International also manufactures an FX series for high frequency LVPECL, LVDS clock de-jitter and frequency translation applications at frequencies such as 125MHz, 156.250MHz.

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