


REV	DESCRIPTION	DATE	PREP	APPD
A	NIR-68518	8/3/17	DF/SM	LT

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 a Knowles company MOUNT HOLLY SPRINGS, PA 17065	Oscillator Specification, Hybrid Clock For Hi-Rel Standard, 300krad Tolerant LVDS
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THE RECORD OF APPROVAL FOR THIS DOCUMENT IS MAINTAINED ELECTRONICALLY WITHIN THE ERP SYSTEM	CODE IDENT NO	SIZE	DWG. NO.	REV
	00136	A	DOC206903	A
UNSPECIFIED TOLERANCES: N/A			SHEET 1 OF 19	

1. SCOPE

- 1.1 General. This specification defines the design, assembly and functional evaluation of high reliability, hybrid clock oscillators produced by Vectron International. Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.
- 1.2 Applications Overview. The designs represented by these products were primarily developed for the MIL-Aerospace community. The lesser Design Pedigrees and Screening Options imbedded within DOC206903 bridge the gap between Space and COTS hardware by providing custom hardware with measures of mechanical, assembly and reliability assurance needed for Military or Ruggedized COTS environments.

2. APPLICABLE DOCUMENTS

- 2.1 Specifications and Standards. The following specifications and standards form a part of this document to the extent specified herein. The issue currently in effect on the date of quotation will be the product baseline, unless otherwise specified. In the event of conflict between the texts of any references cited herein, the text of this document shall take precedence.

Military

MIL-PRF-55310 Oscillators, Crystal Controlled, General Specification For
MIL-PRF-38534 Hybrid Microcircuits, General Specification For

Standards

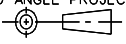
MIL-STD-202 Test Method Standard, Electronic and Electrical Component Parts
MIL-STD-883 Test Methods and Procedures for Microelectronics

Other

DOC206951 Test Specification, Hybrid Clock, Hi-Rel Standard, LVDS Output
QSP-90100 Quality Systems Manual, Vectron International
DOC011627 Identification Common Documents, Materials and Processes, Hi-Rel XO
DOC203982 DPA Specification
QSP-91502 Procedure for Electrostatic Discharge Precautions

3. GENERAL REQUIREMENTS

- 3.1 Classification. All devices delivered to this specification are of hybrid technology conforming to Type 1, Class 2 of MIL-PRF-55310 and have a Class 1C ESDS rating per MIL-PRF-38534. Primarily developed as a Class S equivalent specification, options are imbedded within it to also produce Class B, Engineering Model and Ruggedized COTS devices.
- 3.2 Item Identification. Unique Model Number Series' are utilized to identify device package configurations as listed in Table 1.

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- 3.3 Absolute Maximum Ratings.
- a. Supply Voltage Range (V_{CC}): -0.3Vdc to +4.8Vdc
 - b. Storage Temperature Range (T_{STG}): -65°C to +125°C
 - c. Junction Temperature (T_J): +150°C
 - d. Lead Temperature (soldering, 10 seconds): +300°C

3.4 Design, Parts, Materials and Processes, Assembly, Inspection and Test.

3.4.1 Design. The ruggedized designs implemented for these devices are proven in military and space applications under extreme environments. Designs utilize 4-point crystal mounting in combination with Established Reliability (MIL-ER) components. When specified, radiation hardening up to 300krad(Si) (RHA level F) can be included without altering the device's internal topography.

3.4.1.1 Design and Configuration Stability. Barring changes to improve performance by reselecting passive chip component values to offset component tolerances, there will not be fundamental changes to the design or assembly or parts, materials and processes after first product delivery of that item without written approval from the procuring activity.

3.4.1.2 Environmental Integrity. Designs have passed the environmental qualification levels of MIL-PRF-55310. These designs have also passed extended dynamic levels of at least:

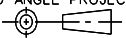
- a. Sine Vibration: MIL-STD-202, Method 204, Condition G (30g pk.)
- b. Random Vibration: MIL-STD-202, Method 214, Condition II-J (43.92g rms, three minute duration in each of three mutually perpendicular directions.)
- c. Mechanical Shock: MIL-STD-202, Method 213, Condition F (1500g, 0.5ms)

3.4.2 Prohibited Parts, Materials and Processes. The items listed are prohibited for use in high reliability devices produced to this specification.

- a. Gold metallization of package elements without a barrier metal.
- b. Zinc chromate as a finish.
- c. Cadmium, zinc, or pure tin external or internal to the device.
- d. Plastic encapsulated semiconductor devices.
- e. Ultrasonically cleaned electronic parts.
- f. Heterojunction Bipolar Transistor (HBT) technology.
- g. 'getter' materials

3.4.3 Assembly. Manufacturing utilizes standardized procedures, processes and verification methods to produce MIL-PRF-55310 Class S / MIL-PRF-38534 Class K equivalent devices. MIL-PRF-38534 Group B Option 1 in-line inspection is included on radiation hardened part numbers to further verify lot pedigree. Traceability of all components and production lots are in accordance with MIL-PRF-38534, as a minimum. Tabulated records are provided as a part of the deliverable data package. Devices are handled in accordance with Vectron document QSP-91502 (Procedure for Electrostatic Discharge Precautions).

3.4.4 Inspection. The inspection requirements of MIL-PRF-55310 apply to all devices delivered to this document. Inspection conditions and standards are documented in accordance with the Quality Assurance, ISO-9001 derived, System of QSP-90100.

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- 3.4.5 Test. The Screening test matrix of Table 5 is tailored for selectable-combination testing to eliminate costs associated with the development/maintenance of device-specific documentation packages while maintaining performance integrity.
- 3.4.6 Marking. Device marking shall be in accordance with the requirements of MIL-PRF-55310.
- 3.4.7 Ruggedized COTS Design Implementation. Design Pedigree “D” devices (see ¶ 5.2) use the same robust designs, component type and construction, found in the other device pedigrees. They do not include the provisions of traceability or the Class-qualified components noted in paragraphs 3.4.3 and 4.1.

4. DETAIL REQUIREMENTS

4.1 Components

4.1.1 Crystals. Cultured quartz crystal resonators are used to provide the selected frequency for the devices. The optional use of Premium Q swept quartz can, because of its processing to remove impurities, be specified to minimize frequency drift when operating in radiation environments. In accordance with MIL-PRF-55310, the manufacturer has a documented crystal element evaluation program.

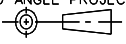
4.1.2 Passive Components. Passive components will have the same pedigree as the die specified in paragraph 7.1. When required, Established Reliability (ER) failure level R minimum passive components are used to the maximum extent possible and procured from QPL suppliers. Lot evaluations are in accordance with MIL-PRF-38534 or Enhanced Element Evaluation as specified in Table 7. When used, inductors will be open construction and may use up to 47 gauge wire.

4.1.3 Class S Active Devices. Devices are assembled with a bipolar transistor and an LVDS chip used to provide the LVDS output. The bipolar semiconductor is procured from wafer lots that have passed MIL-PRF-38534 Class K Lot Acceptance Tests for Class S devices. The LVDS microcircuit die is sourced in accordance with Standard Microcircuit Drawing 5962F9865107V9A, Class V (MIL-PRF-38535) qualified device. All active devices are acceptable for use in environments of up to 300 krad(Si) total dose by Radiation Lot Acceptance Testing of the individual components. ELDRS tolerance on the bipolar transistors is verified by performing an LDR test to 50 krad(Si) and comparing the results to devices from the same lot that were tested at a HDR to 50 krad(Si) and then 300krad(Si). In addition, the bipolar semiconductor is considered insensitive to Single Event Effects and the LVDS output buffer is guaranteed to have no SEL occurrences at an effective LET ≤ 120 MeV-cm²/mg.

4.1.3.1 Class B Active Devices. When specified, active devices assembled into DOC203679 Design Pedigree letters “B” and “C” devices (¶ 5.2a) are procured from wafer lots that have passed MIL-PRF-55310 element evaluations for Class B devices.

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- 4.1.4 Packages. Packages are procured that meet the construction, lead materials and finishes as specified in MIL-PRF-55310. All leads are Kovar with gold plating over a nickel underplate. Package lots are up screened in accordance with the requirements of MIL-PRF-38534 as applicable.
- 4.1.5 Traceability and Homogeneity. All design pedigrees except option D have active device lots that are traceable to the manufacturer's individual wafer; all other elements and materials are traceable to their manufacturer and incoming inspection lots. Design pedigrees E, F, V and X have homogenous material. In addition, swept quartz crystals are traceable to the quartz bar and the processing details of the autoclave lot, as applicable.
- 4.1.6 Enhanced Element Evaluation. When Design Pedigree Option "E" is specified, active and passive devices with Enhanced Element Evaluation as listed in Table 6 and 7 shall be implemented for the highest reliability preference.
- 4.2 Mechanical.
- 4.2.1 Package Outline. Table 1 links each Hi-Rel Standard Model Number of this specification to a corresponding package style. Mechanical Outline information of each package style is found in the referenced Figure.
- 4.2.2 Thermal Characteristics. The calculated thermal resistance and resulting junction temperature rise is found in Table 4.
- 4.3 Electrical.
- 4.3.1 Input Power. Devices are designed for standard +3.3 volt dc operation, $\pm 5\%$. Current is measured, no load, at maximum rated operating Voltage.
- 4.3.2 Temperature Range. Operating range is -55°C to $+125^{\circ}\text{C}$.
- 4.3.3 Frequency Tolerance. Initial accuracy at $+23^{\circ}\text{C}$ is ± 15 ppm maximum. Frequency-Temperature Stability is ± 50 ppm maximum from $+23^{\circ}\text{C}$ reference. Frequency-Voltage Tolerance is ± 4 ppm maximum.
- 4.3.4 Frequency Aging. Aging limits, and when tested in accordance with MIL-PRF-55310 Group B inspection, shall not exceed ± 1.5 ppm the first 30 days, ± 5 ppm Year 1 and ± 2 ppm per year thereafter. When screening Option F is selected, aging is performed on 100% of the lot and Vectron does not apply the PDA as specified in MIL-PRF-55310. Data will be presented for each individual unit to show compliance to the aging limit.
- 4.3.4.1 Frequency Aging Duration Option. By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than half of the specified aging rate. This is a common method of expediting 30-Day Aging without incurring risk to the hardware and used quite successfully for numerous customers. It is based on the 'least squares fit' determinations of MIL-PRF-55310 paragraph 4.8.35. The 'half the time/half the spec' limit is generally conservative as roughly 2/3 of a unit's Aging deviation occurs within that period of time.

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Vectron's automated aging systems take about 6 data points per day, so a lot of data is available to do very accurate projections, much more data than what is required by MIL-PRF-55310. The delivered data would include the Aging plots projected to 30 days. If the units would not perform within that limit then they would continue to full 30 Day term. Please advise by purchase order text if this may be an acceptable option to exercise as it assists in Production Test planning.

4.3.5 Operating Characteristics. Symmetrical square wave limits are dependent on the device frequency and are in accordance with Table 2 and Figure 1. Start-up time is 10.0 msec. maximum.

4.3.6 Output Load. See Figure 2.

5. QUALITY ASSURANCE PROVISIONS AND VERIFICATION

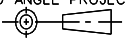
5.1 Verification and Test. Device lots shall be tested prior to delivery in accordance with the applicable Screening Option letter as stated by the 15th character of the part number. Table 5 tests are conducted in the order shown and annotated on the appropriate process travelers and data sheets of the governing test procedure. For devices that require Screening Options that include MIL-PRF-55310 Group A testing, the Post-Burn-In Electrical Test and the Group A Electrical Test are combined into one operation.

5.1.1 Screening Options. The Screening Options, by letter, are summarized as:

- A Modified MIL-PRF-38534 Class K
- B Modified MIL-PRF-55310 Class B Screening & Group A Quality Conformance Inspection (QCI)
- C Modified MIL-PRF-55310 Class S Screening & Group A QCI
- D Modified MIL-PRF-38534 Class K with Group B Aging
- E Modified MIL-PRF-55310 Class B Screening, Groups A & B QCI
- F Modified MIL-PRF-55310 Class S Screening, Groups A & B QCI
- G Modified MIL-PRF-55310 Class B Screening & Post Burn-in Nominal Electricals
- X Engineering Model (EM)

5.2 Optional Design, Test and Data Parameters. The following is a list of design, assembly, inspection and test options that can be selected or added by purchase order request.

- a. Design Pedigree (choose one as the 5th character in the part number):
 - (E) Enhanced Element Evaluation, 300krad Class S die, Premium Q Swept Quartz
 - (F) Hi-Rel design w/ 300krad Class S die, Premium Q Swept Quartz
 - (V) Hi-Rel design w/ 300krad Class S die, Non-Swept Quartz
 - (X) Hi-Rel design w/ Non-Swept Quartz, Class S die
 - (B) Hi-Rel design w/ Swept Quartz, Class B die
 - (C) Hi-Rel design w/ Non-Swept Quartz, Class B die
 - (D) Hi-Rel design w/ Non-Swept Quartz and commercial grade components
- b. Input Voltage, (B) for +3.3V as the 14th character
- c. Frequency-Temperature Slew Test
- d. Radiographic Inspection

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- e. Group C Inspection: In accordance with MIL-PRF-55310, Table VII (requires 8 destruct specimens)
- f. Group C Inspection: In accordance with MIL-PRF-38534, Table C-Xc, Condition PI (requires 8 destruct specimens – 5 pc. Life, 3 pc. RGA) Subgroup 1 fine leak test to be performed per MIL-STD-202, Method 112, Test Condition C.
- g. Qualification: In accordance with EEE-INST-002, Section C4, Table 3, Level 1 or 2 (requires 11 destruct specimens)
- h. Internal Water-Vapor Content (RGA) samples and test performance
- i. MTBF Reliability Calculations
- j. Worst Case/Derating Analysis
- k. Deliverable Process Identification Documentation (PID)
- l. Customer Source Inspection (pre-crystal mount pre-cap, post-crystal mount pre-cap and final). Due to components being mounted underneath the crystal blank, pre-crystal mount pre-cap inspection should be considered.
- m. Destruct Physical Analysis (DPA): MIL-STD-1580 with exceptions as specified in Vectron DOC203982.
- n. Qualification: In accordance with MIL-PRF-55310, Table IV (requires 11 destruct specimens).
- o. High Resolution Digital Pre-Cap Photographs (20 Megapixels minimum)
- p. Hot solder dip of leads with Sn63/Pb37 solder prior to shipping

5.2.1 NASA EEE-INST-002. A combination of Design Pedigree E or R, Option F Screening, Group C Inspection in accordance with Table VII of MIL-PRF-55310 and RGA, meet the requirements of Level 1 device reliability. A combination of Design Pedigree B, Option E Screening, Radiographic Inspection, Group C Inspection in accordance with Table VII of MIL-PRF-55310 and RGA, meet the requirements of Level 2 device reliability.

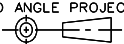
5.3 Test Conditions. Unless otherwise stated herein, inspections are performed in accordance with those specified in MIL-PRF-55310 and MIL-PRF-38534, in that order. Process travelers identify the applicable methods, conditions and procedures to be used. Examples of electrical test procedures that correspond to MIL-PRF-55310 requirements are shown in Table 3.

5.4 Special Test and Description.

5.4.1 Frequency-Temperature Slew. Frequency-Temperature Slew Test has been developed as an indicator of higher than normal internal water vapor content. The incremental temperature sweep from +125°C to -55°C and back to +125°C records output frequency fluctuations emulating the mass loading of moisture deposited on the crystal blank surface. Though not replacing a customer’s internal water-vapor content (RGA) requirement, confidence is increased without destructively testing otherwise good devices.

5.5 Deliverable Data. The manufacturer supplies the following data, as a minimum, with each lot of devices:

- a. Completed assembly and screening lot travelers, including rework history and Certificate of Conformance.
- b. Electrical test variables data, identified by unique serial number.

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- c. Frequency-Temperature Slew plots, Radiographic films, Group C data and RGA data as required by purchase order.
- d. Traceability, component LAT, enclosure LAT and RLAT (if specifically requested on the purchase order).

5.6 Discrepant Material. All MRB authority resides with the procuring activity.

5.7 Failure Analysis. Any catastrophic failure (no clocking, no current) at Post Burn-In or after will be evaluated for root cause. The customer will be notified after occurrence and upon completion of the evaluation.

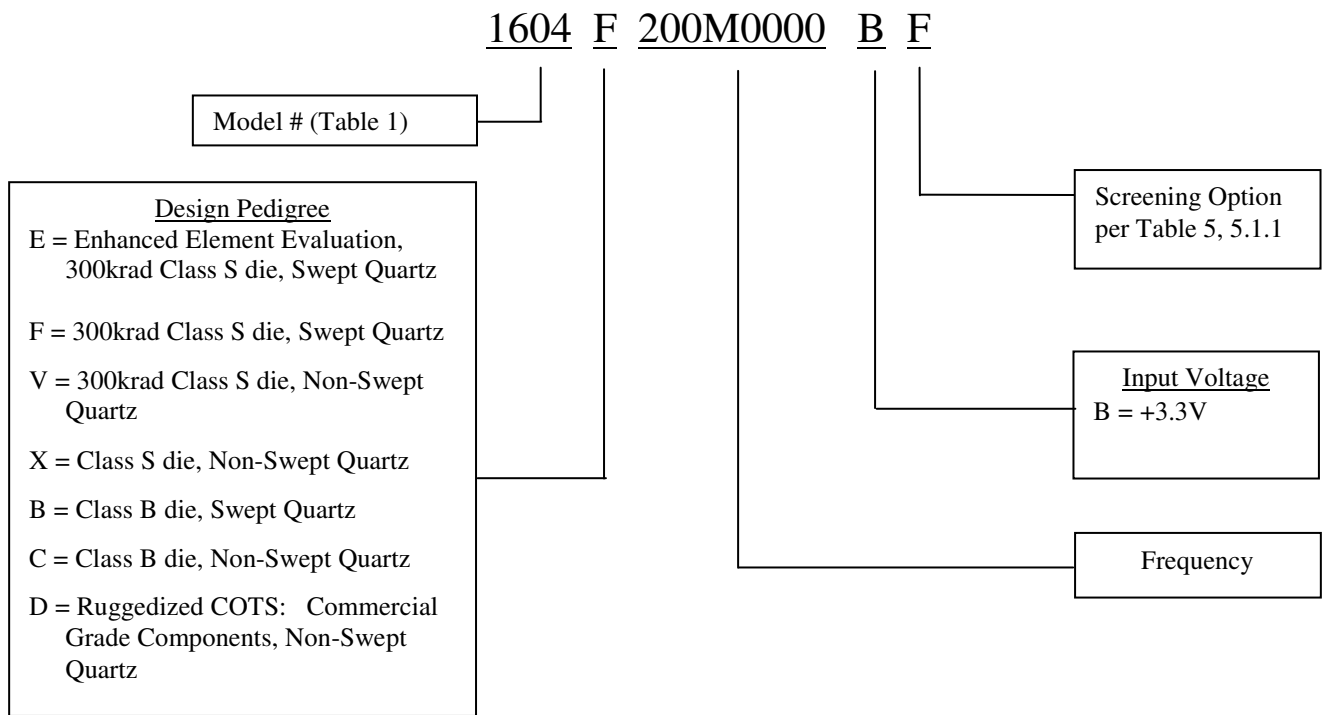
6. PREPARATION FOR DELIVERY

6.1 Packaging. Devices will be packaged in a manner that prevents handling and transit damage during shipping. Devices will be handled in accordance with MIL-STD-1686 for Class 1 devices.

7. ORDERING INFORMATION

7.1 Ordering Part Number. The ordering part number is made up of an alphanumeric series of 15 characters. Design-affected product options, identified by the parenthetic letter on the Optional Parameters list (§ 5.2a and b), are included within the device part number.

The Part Number breakdown is described as:



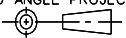
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- 7.1.1 Model Number. The device model number is the four (4) digit number assigned to a corresponding package and output combination per Table 1.
- 7.1.2 Design Pedigree. Class S variants correspond to either letter “E”, “F”, “V” or “X” and are described in paragraph 5.2a. Class B variants correspond to either letter “B” or “C” and are described in paragraph 5.2a. Ruggedized COTS, using commercial grade components, corresponds to letter “D”.
- 7.1.3 Output Frequency. The nominal output frequency is expressed in the format as specified in MIL-PRF-55310 utilizing eight (8) characters.
- 7.1.4 Input Voltage. Voltage is the 14th character, letter “B” represents +3.3V.
- 7.1.5 Screening Options. The 15th character is the Screening Option (letter A thru G or X) selected from Table 5.
- 7.2 Optional Design, Test and Data Parameters. Test and documentation requirements above that of the standard high reliability model shall be specified by separate purchase order line items (as listed in ¶ 5.2c thru p).

MODEL #	PACKAGE	OUTPUT (LVDS)	MECHANICAL OUTLINE AND I/O CONNECTIONS
1604	20 Lead Flatpack	Single Pair	Figure 3
1620 <u>1</u> /	20 Lead Flatpack	Single Pair	Figure 4
1608	20 Lead Flatpack	Dual Pairs	Figure 3
1640 <u>1</u> /	20 Lead Flatpack	Dual Pairs	Figure 4
1616	20 Lead Flatpack	Quad Pairs	Figure 3
1680 <u>1</u> /	20 Lead Flatpack	Quad Pairs	Figure 4

1/. Models 1620, 1640 and 1680 are lead formed versions of Models 1604, 1608 and 1616 respectively. See Appendix A for recommended land pattern.

TABLE 1 - Item Identification and Package Outline

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Frequency Range @ 3.3V Operation: 12 MHz to 200 MHz <u>1/</u>					
Temperature Range: -55°C to +125°C					
Frequency Tolerance, Initial Accuracy @ +23°C: ±15 ppm max.					
Frequency-Temperature Stability from +23°C ref.: ±50 ppm max.					
Frequency-Voltage Tolerance: ±4 ppm max. (Vcc ± 5%)					
Frequency Aging: ±1.5 ppm max. 1st 30 days, ±5 ppm max. Year 1, ±2 ppm max. Year 2+					
Start-up Time: 10.0 ms max.					
Differential Output Voltage VOD: 250mV to 400mV					
Offset Voltage VOS: 1.125V to 1.450V					
Frequency Range (MHz)	Single Pair Current <u>2/</u> (mA max)	Dual Pairs Current <u>2/</u> (mA max)	Quad Pairs Current <u>2/</u> (mA max)	Rise/Fall Times (ps max)	Duty Cycle (%)
12 – 50	15	28	35	600	40 to 60
> 50 – 100	20	30	40	600	40 to 60
> 100 – 160	25	40	45	600	40 to 60
> 160 – 200	30	45	45	600	40 to 60

1/. Waveform measurement points and logic limits are in accordance with Figure 1.

2/. Current measurements are taken with no load at maximum supply voltage.

TABLE 2 - Electrical Performance Characteristics

Frequency Range (MHz)	Typical Period Jitter 1 sigma (ps)	Typical Period Jitter peak-to-peak (ps)	Phase Jitter 12kHz to 20MHz (ps)
12	3.5	30	2.652
30	3.5	30	0.752
40	3.5	30	0.448
60	3.5	30	0.269
80	3.5	30	0.212
100	2.5	22	0.200
125	2.5	22	0.145
156.25	2.5	22	0.115
200	2.5	22	0.090

TABLE 2a – Typical Jitter Performance

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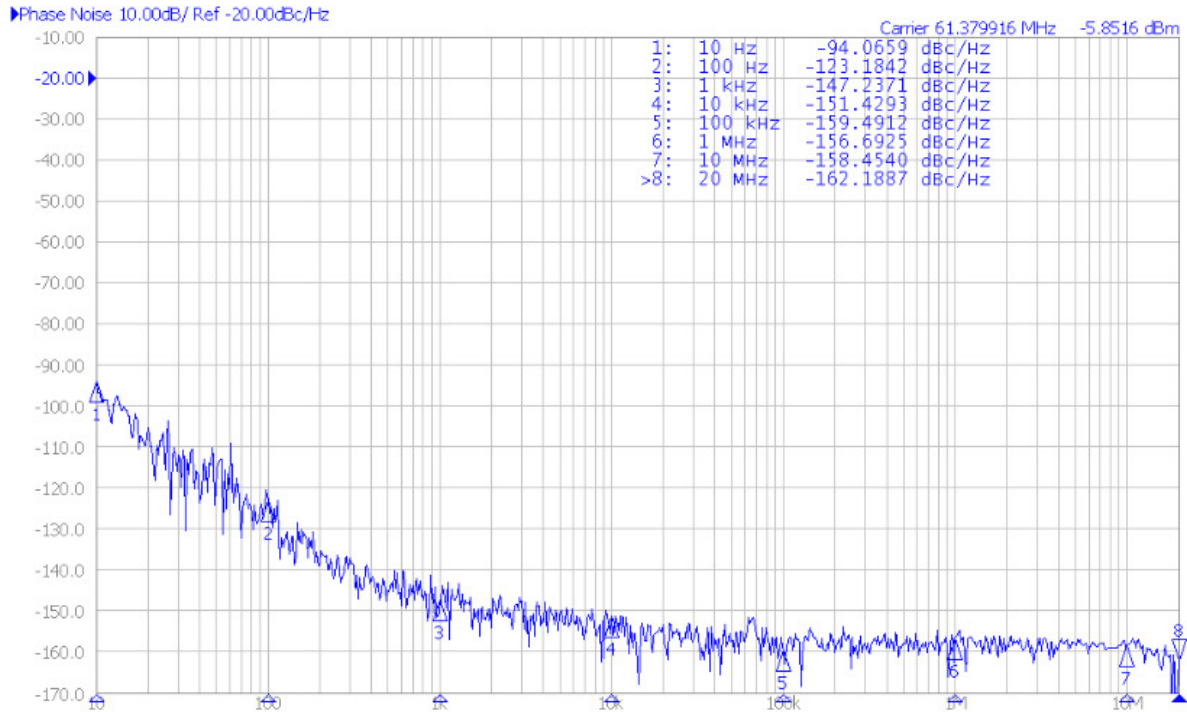


TABLE 2b – Typical Phase Noise Performance at 61.380 MHz, Quad Pair

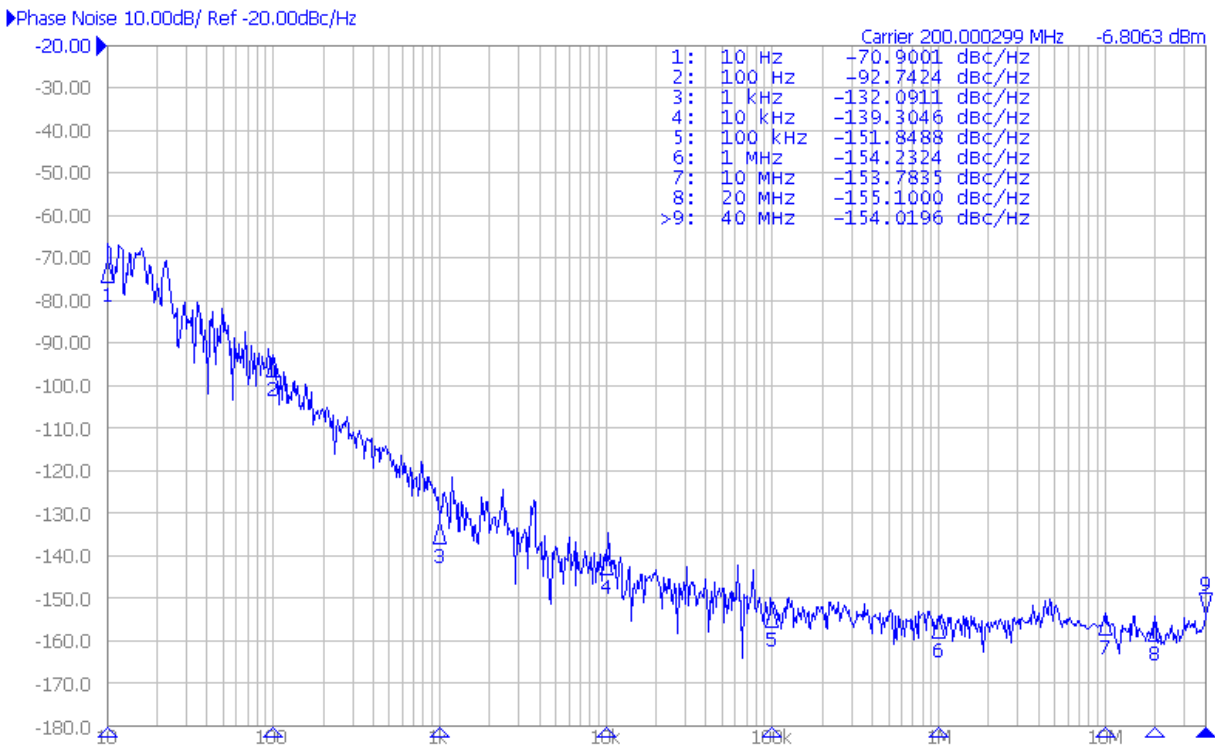
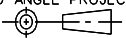


TABLE 2c – Typical Phase Noise Performance at 200.000 MHz, Dual Pair

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OPERATION LISTING	REQUIREMENTS AND CONDITIONS <u>1/</u>
@ all Electrical tests	
Input Current (no load)	MIL-PRF-55310, Para 4.8.5.1
Initial Accuracy @ Ref. Temp.	MIL-PRF-55310, Para 4.8.6
Output Logic Voltage Levels	MIL-PRF-55310, Para 4.8.21.3
Rise and Fall Times	MIL-PRF-55310, Para 4.8.22
Duty Cycle	MIL-PRF-55310, Para 4.8.23
@ Post Burn-In Electrical only	
Overvoltage Survivability	MIL-PRF-55310, Para 4.8.4
Initial Freq. – Temp. Accuracy	MIL-PRF-55310, Para 4.8.10.1
Freq. – Voltage Tolerance	MIL-PRF-55310, Para 4.8.14
Start-up Time (fast/slow start)	MIL-PRF-55310, Para 4.8.29

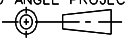
1/. Waveform measurement points and logic limits are in accordance with Figure 1.

TABLE 3 - Electrical Test Parameters

Thermal Resistance Junction to Case θ_{jc} (°C / W)	Δ Junction Temp. T_j (°C @ max. power)	Typical Weight (Grams)
22.1	3.44	3.0

Note: The maximum power from Table 2 is used to calculate the worst case Δ junction temperature.

TABLE 4 - Thermal Characteristics

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OPN. NO.	OPERATION LISTING	REQUIREMENTS AND CONDITIONS	Option A	Option B	Option C	Option D	Option E	Option F	Option G	Option X
	SCREENING	MIL Class Similarity	K	B-	S-	K+	B	S		EM
			100%	100%	100%	100%	100%	100%	100%	100%
1	Non-Destruct Bond Pull	MIL-STD-883, Meth 2023	X	NR	X	X	NR	X	NR	NR
2	Internal Visual	MIL-STD-883, Meth 2017 Class K, Meth 2032 Class K	X	X	X	X	X	X	X	X
3	Stabilization (Vacuum) Bake	MIL-STD-883, Meth 1008, Cond C, 150°C	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 48 hrs.	X 24 hrs.	X 48 hrs.	X 24 hrs.	X 24 hrs.
4	Thermal Shock	MIL-STD-883, Meth 1011, Cond A	NR	NR	X	NR	NR	X	NR	NR
5	Temperature Cycle	MIL-STD-883, Meth 1010, Cond. B, 10 cycles min.	X	X	X	X	X	X	X	NR
6	Constant Acceleration	MIL-STD-883, Meth 2001, Cond A, Y1 plane only, 5000 g's	X	X	X	X	X	X	X	NR
7	Particle Impact Noise Detection	MIL-STD-883, Meth 2020, Cond B	X	X	X	X	X	X	NR	X
8	Electrical Testing, Pre Burn-In	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	X	X	X	X	X	X	X
9	1 st Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	X 160 hrs.	X 240 hrs.	X 160 hrs.	NR
10	Electrical Testing, Intermediate	Perform tests in Table 3. Nominal Vcc, nominal temperature	X	NR	NR	X	NR	NR	NR	NR
11	2 nd Burn-In	MIL-STD-883, Meth 1015, Condition B	X 160 hrs.	NR	NR	X 160 hrs.	NR	NR	NR	NR
12	Freq-Temp Slew Test	Operating temp. range, frequency plotted at 1.0°C steps	AR	AR	AR	AR	AR	AR	NR	NR
13	Electrical Testing, Post Burn-In (Group A)	Perform tests in Table 3. Nominal Vcc & extremes, nominal temperature & extremes	X	X	X	X	X	X	X nom. Vcc	NR
14	Seal: Fine Leak	MIL-STD-202, Meth 112, Cond C 5 x 10 ⁻⁸ atm cc/sec max	X	X	X	X	X	X	X	X
15	Seal: Gross Leak	MIL-STD-202, Meth 112, Cond D	X	X	X	X	X	X	X	X
16	Radiographic Inspection	MIL-STD-883, Meth 2012	X	AR	AR	X	AR	X	NR	NR
17	Solderability	MIL-STD-883, Meth 2003	<u>1/</u>	<u>1/</u>	<u>1/</u>	<u>1/</u>	<u>1/</u>	<u>1/</u>	<u>1/</u>	NR
18	External Visual & Mechanical	MIL-STD-883, Meth 2009	X <u>2/</u>	X <u>2/</u>	X <u>2/</u>	X <u>2/</u>	X <u>2/</u>	X <u>2/</u>	X <u>2/</u>	X <u>2/</u>
19	Aging, 30 Day <u>3/</u> (M55310 Group B)	MIL-PRF-55310, para. 4.8.35.1	NR	NR	NR	X	13 pcs.	X	NR	NR

LEGEND: X = Required, NR = Not Required, AR = As Required

TABLE 5 – Test Matrix

1/ Performed at package LAT. Include LAT data sheet.

2/ When specified, RGA samples will be removed from the lot after completion of this operation. Use of Screening failures requires customer concurrence.

3/ By customer request, the Aging test may be terminated after 15 days if the measured aging rate is less than one-half the specified aging rate, as described in paragraph 4.3.4.1 herein. See the customer PO.

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Subgroup	Class K	Test	Mil-STD-750		Quantity (accept number)	Mil-PRF-38534 Reference Paragraph
			Method	Condition		
1	X	Element Electrical A. May perform at wafer level B. All failures shall be removed from the lot		Perform at room ambient	100%	C.3.3.1
2	X	Element Visual	2069, 2070, 2072, 2073		100%	C.3.3.2
3	X	Internal Visual	2069, 2070, 2072, 2073, 2074		10(0) or 22(0) (Notes 1 & 2)	C.3.3.3 C.3.3.4.2
4	X	Temperature Cycling	1051	C	10(0) 22(0) (See Notes 1 & 2)	C.3.3.3
	X	Surge Current (when applicable)	4066	A or B as specified		
	X	Constant Acceleration	2006 2001	Y1 direction 20,000 G / 10,000 G for Pd ≥ 10W		
	X	Interim Electrical				C.3.3.4.3
	X	High Temperature Reverse Bias (HTRB)	1039 1042 1038	A B A		
	X	Interim Electrical & Delta		Complete Within 16 hrs of HTRB completion		
	X	Burn-In 240 hours	1039, 1042 1038 1040	B A B		
	X	Post Burn-In Electrical				C.3.3.4.3
	X	Steady State Life 1000 hours	1026 1037 1042 1048			
	X	Final Electrical				C.3.3.4.3
5	X	Wire Bond Evaluation	2011		10(0) wires or 20(1) wires	C.3.3.3 C.3.3.5
6	X	SEM	2018 2077		See method 2018 or 2077 & Note 2	C.3.3.6

NOTES:

- Subgroups 3, 4, & 5 shall be performed on a sample of 10 die if the wafer lot is from a QPL/QML line. If the die are from commercial wafer lots, then the sample size shall be 22 die. Die from QPL/QML wafers not meeting the QPL/QML requirements and downgraded to commercial grade shall not be used.
- Subgroups 3, 4 & 5 shall be performed in the order listed in Table 1. Subgroup 6 may be performed at any time.

TABLE 6 - SEMICONDUCTOR ENHANCED ELEMENT EVALUATION

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Parts Type	Test	Requirement Paragraph	Sample size	Allowable Reject(s)
Ceramic Capacitors				
M55681 FRL S or M123 (chips)	N/A	N/A	N/A	N/A
COTS (chips)	Ultrasonic Scan or CSAM	M123	100%	N/A
	Group A	M123	M123	M1233
	Group B, Subgroups 1 and 2	M123	M123	M123
Resistors				
M55342 FRL R or S	N/A	N/A	N/A	N/A
COTS	Group A	M55342 Table IX, Subgroups 1,2 and 3	M55342 for T-level	M55342 for T-level
	Group B	M55342 Table XI, Subgroups 1 and 2	M55342 for T-level	M55342 for T-level
Inductors (See Paragraph 4.1.2)				
Custom closed magnetics	Group A	MIL-STD-981	MIL-STD-981	MIL-STD-981
	Group B	MIL-STD-981	MIL-STD-981	MIL-STD-981
<p>Magnetics, Closed Construction Leaded and Surface Mount (transformers, inductors, coils) (Note: Stacking magnetics shall be qualified and the effects of the long term performance of the hybrids verified. When stacking magnetics, a repeat of the thermal cycling plus electrical measurements as specified in Group A of MIL-STD-981. Design, workmanship and materials/processes shall conform to MIL-STD-981 requirements).</p> <p>Magnetics, Open Construction are unencapsulated and unpotted self-leaded parts consisting of magnet wire wound around a magnetic core. These parts are fully visually inspectable. Open construction magnetics shall be subjected to 100% electrical measurements and visual inspection per MIL-STD-981.</p>				

TABLE 7: PASSIVE COMPONENT ENHANCED ELEMENT EVALUATION

SIZE A	CODE IDENT NO. 00136	THIRD ANGLE PROJECTION 	UNSPECIFIED TOLERANCES N/A	DWG NO. DOC206903	REV. A	SHEET 15
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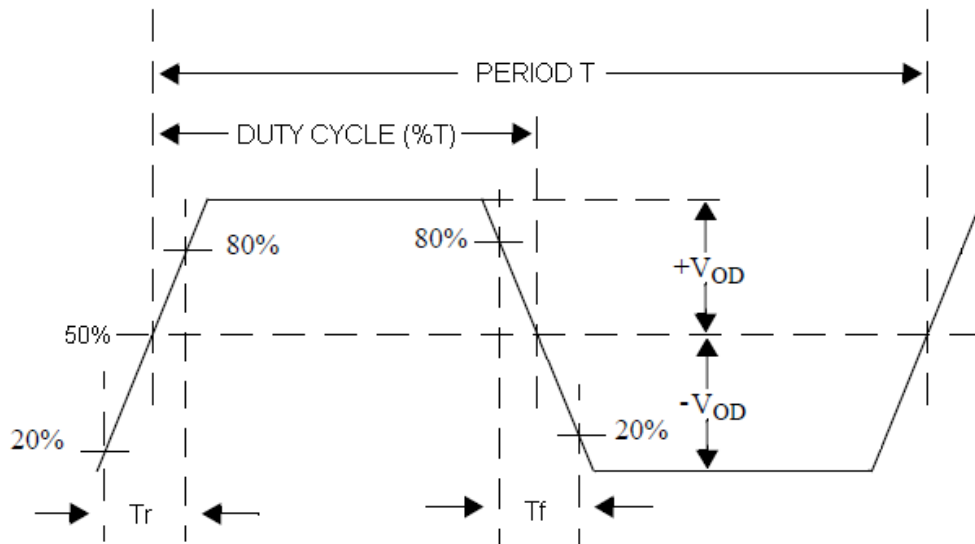


FIGURE 1
Differential Output Waveform

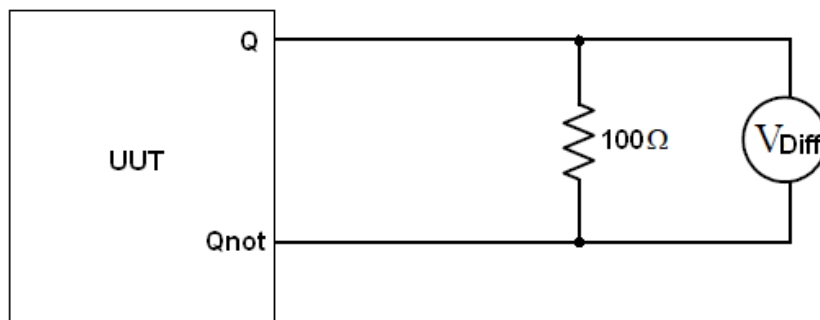
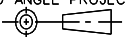
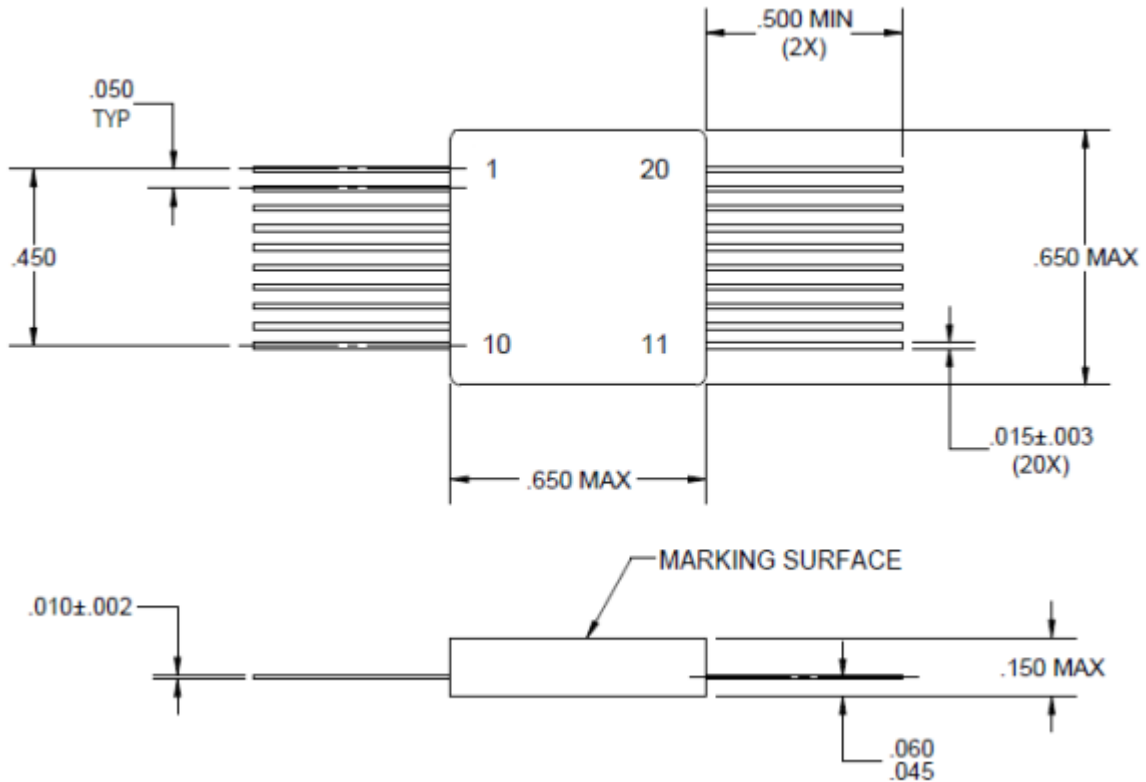


FIGURE 2
Output Load, 100Ω between outputs

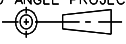
SIZE A	CODE IDENT NO. 00136	THIRD ANGLE PROJECTION 	UNSPECIFIED TOLERANCES N/A	DWG NO. DOC206903	REV. A	SHEET 16
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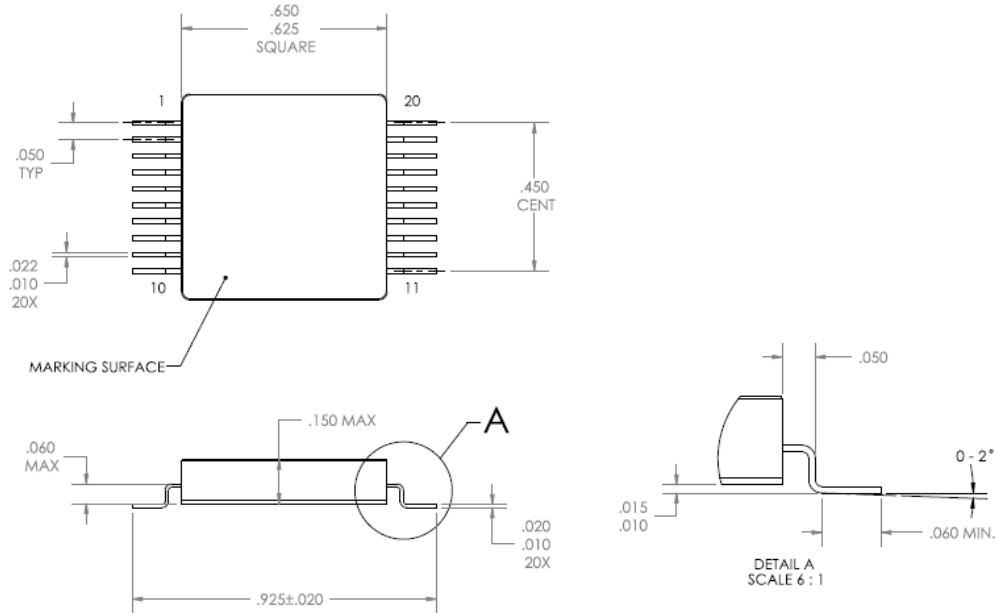


Model #	I/O Connections										
	Vcc	Q1	$\bar{Q}1$	Q2	$\bar{Q}2$	Q3	$\bar{Q}3$	Q4	$\bar{Q}4$	Enable <u>1/</u>	Gnd/Case
1604	13,20	11	12	-	-	-	-	-	-	-	10
1608	20	11	12	14	15	-	-	-	-	13	10
1616	20	7	8	10	9	11	12	14	13	-	6,15

1/ Outputs are enabled when Pin 13 is left floating or 0V to 0.8V is applied. Outputs are disabled (high impedance) when 2.0V to Vcc is applied.

FIGURE 3
Model 1604/1608/1616 Package Outline and I/O Connections

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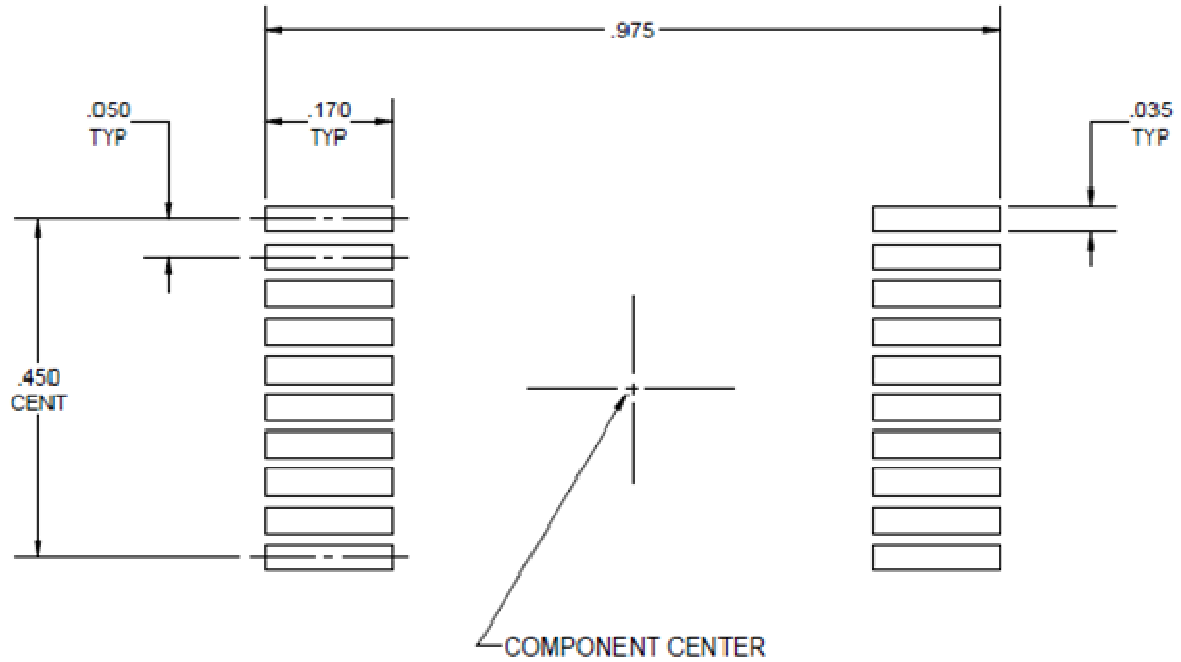
Model #	I/O Connections										
	Vcc	Q1	$\bar{Q}1$	Q2	$\bar{Q}2$	Q3	$\bar{Q}3$	Q4	$\bar{Q}4$	Enable <u>1/</u>	Gnd/Case
1620	13,20	11	12	-	-	-	-	-	-	-	10
1640	20	11	12	14	15	-	-	-	-	13	10
1680	20	7	8	10	9	11	12	14	13	-	6,15

1/ Outputs are enabled when Pin 13 is left floating or 0V to 0.8V is applied. Outputs are disabled (high impedance) when 2.0V to Vcc is applied.

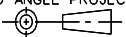
FIGURE 4
Model 1620/1640/1680 Package Outline and I/O Connections

SIZE A	CODE IDENT NO. 00136	THIRD ANGLE PROJECTION 	UNSPECIFIED TOLERANCES N/A	DWG NO. DOC206903	REV. A	SHEET 18
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APPENDIX A
Recommended Land Pattern



Models 1620, 1640 and 1680

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